



ELECTRICAL & COMPUTER ENGINEERING DEPARTMENT



THESIS DEFENCE

Friday, November 8th, 2002

12:40 – 1:40 pm

Room 719

Engineering & Architecture Building

DESIGN AND IMPLEMENTATION OF A DSP CORE ON THE WDC 65C816 MICROPROCESSOR

Ajay Kumar Yadav

**Department of Electrical and Computer Engineering
Temple University**

Advisor: Dr. Dennis Silage

Digital Signal Processing (DSP) applications are becoming increasingly dependent on complex heterogeneous architectures, featuring a combination of a general-purpose microprocessor and DSP application specific processor. The key advantage of such architectures is their ability to arrange the data computation between the processors on the basis of applications. This Thesis focuses on the implementation of a DSP processor core as a seamless adjunct to the 16-bit WDC 65C816 general-purpose microprocessor. The Thesis evaluates the available 16-bit fixed point DSP architectures and presents a design of the compatible DSP processor core. The Thesis also specifies the architectural changes of the WDC 65C816 architecture and describes the advantages of the new added features. DSP filter algorithms are implemented on the designed architecture to test its performance and to provide comparative benchmarks. The Verilog HDL code of the DSP core integrated with the modified WDC 65C816 microprocessor is simulated in the Simucad Silos 2001 environment and synthesized using Cypress Semiconductor Warp. The processor latency and data throughput has been tested and verified in the Aldec Active HDL-Sim. This work is supported by the System Chip Design Center (www.temple.edu/scdc).

ALL ARE INVITED TO ATTEND